REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of October 14, 2008 (hereinafter "Office Action"). In response, Applicants have amended independent Claims 1, 8, and 14 to clarify that the recited clock circuits receive one or more error signals at input(s) thereof. Various dependent claims have been amended to be consistent with the amendments to independent Claims 1, 8, and 14. Claims 19 – 24 have been canceled without prejudice or disclaimer. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Interview Summary

Applicants wish to thank the Examiner for discussing the pending claims with Applicants' representative, Scott Moore (Reg. No. 42,011) on February 13, 2009. During the interview, Applicants' representative stated that the independent Claims 1, 8, and 14 may be amended as indicated above; however, no agreement was reached as to the patentability of the pending independent claims as amended. Applicants respectfully request that the present remarks constitute an Interview Summary pursuant to MPEP §713.04.

Independent Claims 1, 8, and 14 are Patentable

Independent Claims 1, 8, and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 5,146,585 to Smith, III (hereinafter "Smith"). (Office Action, page 2).

Independent Claim 1 is directed to a clock distribution circuit and includes the following recitations:

> a first clock circuit that is configured to generate a first clock signal responsive to an error signal received at an input thereof;
>
> a second clock circuit that is configured to generate a second clock

> signal responsive to the error signal received at an input thereof; and
> a phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive to the first and the second clock signals. (Emphasis added).

Independent Claims 8 and 14 include similar recitations. According to the recitations of Claim 1, first and second clock circuits generate respective clock signals responsive to the same error signal, which is generated by a phase detector circuit that connects the first and second clock circuits. Moreover, each of the first and second clock circuits receives the error signal at an input thereof.

In rejecting Claim 1, the Office Action cites the Time-Of –Day (TOD) synchronization system shown in FIG. 1 of Smith in which two clock sources 12a and 12b are alleged to correspond to the recited first and second clock circuits. (Office Action, pages 2 and 3). Smith shows two clock sources 12a and 12b that generate respective error signals based on their own output clock signal and the other clock source's output clock signal (Smith, FIG. 1, links 14 and 16) using respective internal phase comparator circuits. (Smith, FIG. 2, phase comparator 38). Each of the clock sources 12a and 12b uses the error signal generated internally by the phase comparator circuit 38 to drive a voltage controlled oscillator circuit 28 (Smith, FIG. 2), which generates an internal clock output signal on line 44. The internal clock output signal is further processed by a divider circuit 30 (Smith, FIG. 2) and an encoder/transmitter circuit 32 (Smith, FIG. 2) to generate the output signal on line 46. Applicants agree that Smith's TOD synchronization system shown in FIG. 1 can be interpreted as teaching two clock circuits that generate first and second clock signals, respectively, responsive to a common error signal. For example, the first clock source 12a generates an output clock signal responsive to an internally generated error signal based on its own output clock signal and the output signal of the second clock source 12b. The second clock source 12b generates an output signal responsive to an internally generated error signal based on its own output clock signal and the output signal of the first clock source 12a. Thus, the first and second clock sources 12a and 12b generate first and second output clock signals, respectively, responsive to a common error signal generated based on the first and second

output clock signals, where the common error signal may be either of the error signals generated by the phase comparator circuit 38 in the respective first and second clock sources 12a and 12b.

In sharp contrast to the TOD synchronization system of Smith, independent Claim 1 has been amended to clarify that each of the first and second clock circuits receives the error signal at an input thereof. As shown in FIG. 1 of Smith, each of the first and second clock sources 12a and 12b receives the output clock signal from the other clock source as an input on line 16 or line 14. The first and second clock sources 12a and 12b do not receive a common error signal at respective inputs thereof as each of the clock sources 12a and 12b generates an internal error signal using the phase comparator circuit 38 (Smith, FIG. 2) and the output signal from the phase comparator circuit 38 from one of the first and second clock sources 12a and 12b is not used as an input to the other one of the first and second clock sources 12a and 12b.

Applicants further note that in rejecting independent Claim 1, the Office Action alleges that it would be obvious to incorporate one of the first and second clock sources 12a and 12b into the other clock source so that only one error signal is generated by the phase comparator circuit 38. (Office Action, page 3). By merging the two clock sources 12a and 12b of Smith into one clock source, however, the modified system does not disclose two clock circuits as recited in independent Claim 1. If the Office Action is alleging that the two clock sources 12a and 12b could share a common phase comparator 38, then this would appear to degrade the performance of Smith's TOD synchronization system as the phase comparator 38 would need to be time shared as it could not generate an error signal for one clock source 12a at the same time it is generating an error signal for the other clock source 12b. By definition, the time-shared common phase comparator 38 would not be able to generate a common error signal, much less one that is received at respective inputs of the two clock sources 12a and 12b.

Applicants submit, therefore, that independent Claim 1 is patentable as Smith fails to disclose or suggest first and second clock circuits that generate respective clock signals responsive to the same error signal, which is generated by a phase detector circuit that

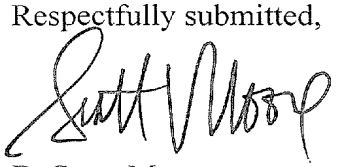
connects the first and second clock circuits, and which is received at respective inputs of the first and second clock circuits. The Office Action rejects independent Claims 8 and 14 using the same rationale to reject independent Claim 1. (Office Action, pages 4 and 5). Applicants submit that independent Claims 8 and 14 are patentable for at least the reasons discussed above with respect to independent Claim 1

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 8, and 14 are patentable over Smith and that Claims 2 - 7, 9 - 13, and 15 - 18 are patentable at least per the patentability of independent Claims 1, 8, and 14.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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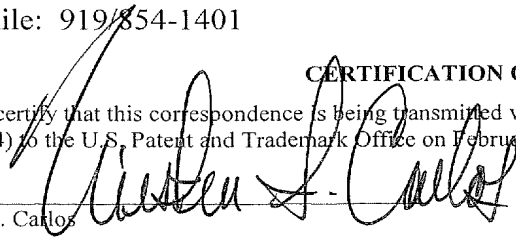

Kirsten S. Carlos